EE108 Final Planning Document — Taylor Tam, Benji Warburton, Danica Sun

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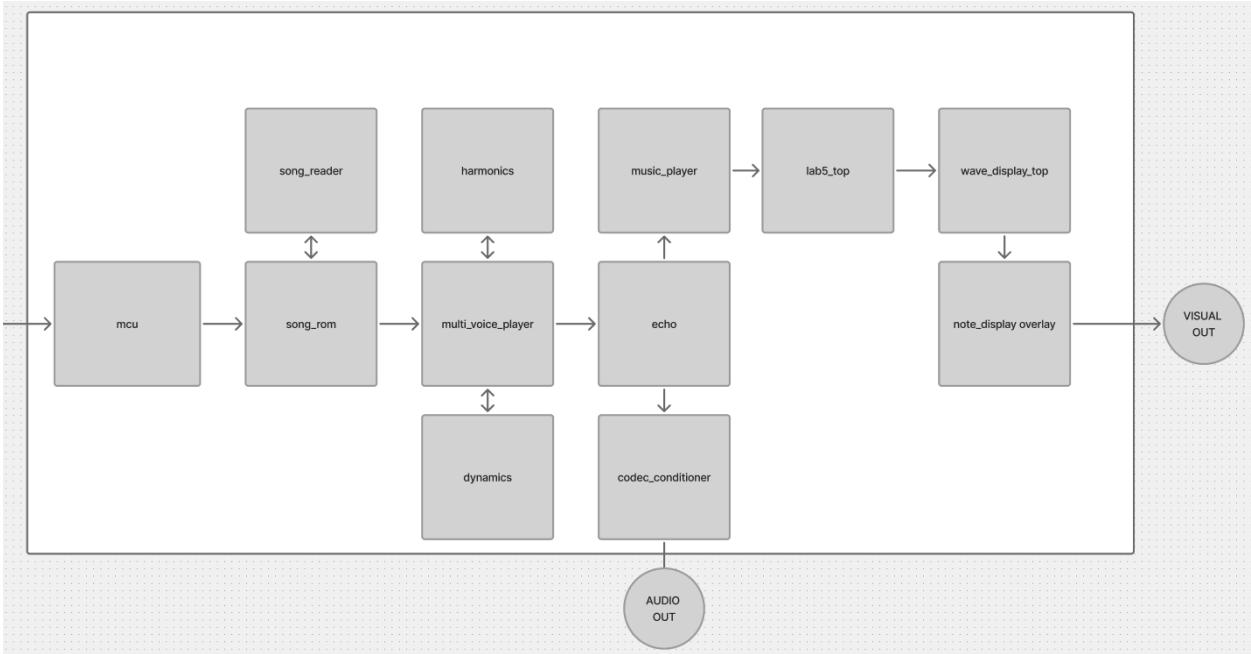
High-Level Implementation

The MCU selects the song to be played, and the song_reader steps through the song note-by-note by fetching data from song_rom. Each note is synthesized in the audio path, where harmonics enriches the waveform, dynamics applies an ASDR envelope, and multi_voice_player combines the voices into a multi-chorded output. These are passed to echo, which adds a delayed, attenuated copy using a circular buffer. We can read songs from ROM, play up multiple simultaneous harmonically shaped notes with ASDR dynamics, and output the resulting audio to codec while displaying past, present, and future notes on a display.



Module Specifications

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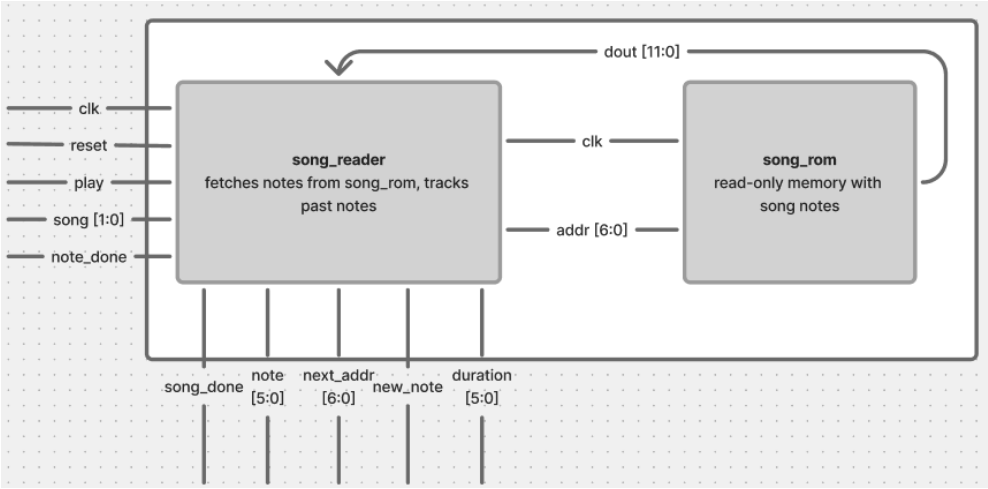
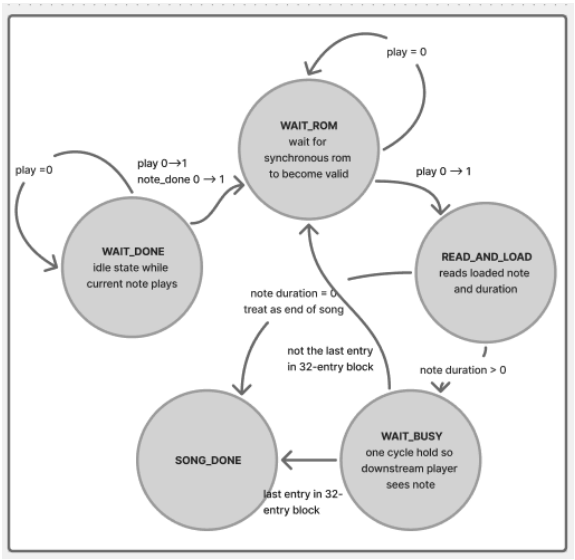
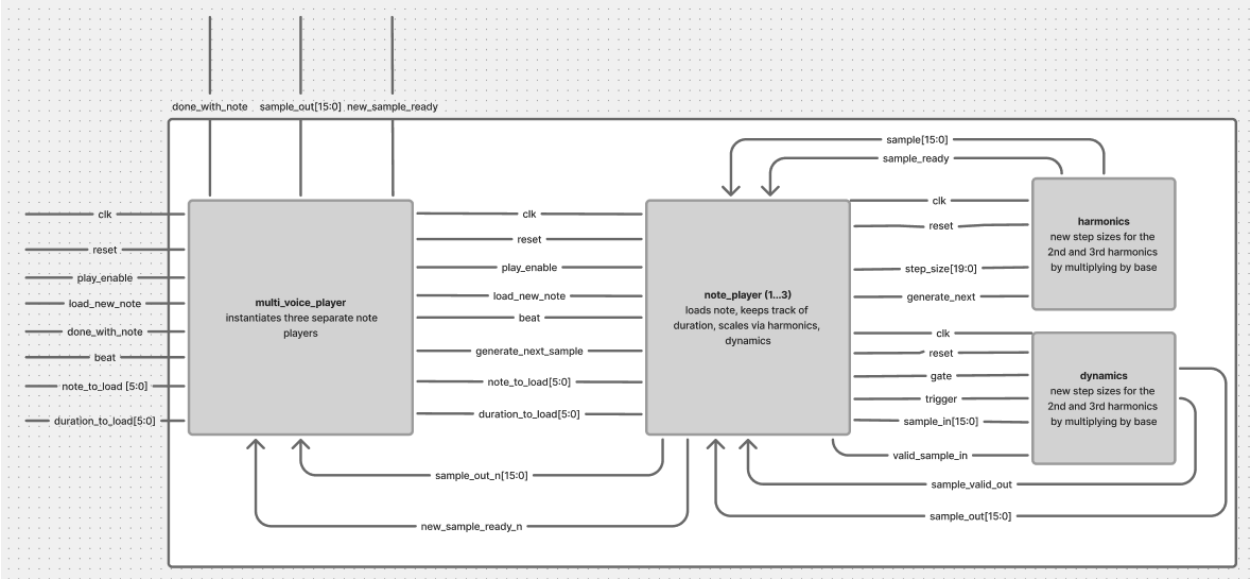
1 – Chords (4 points)

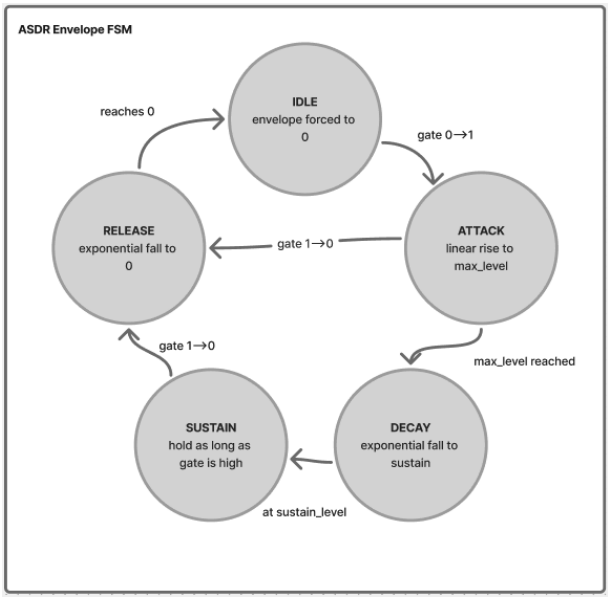




This controlled how notes were fetched from song_rom and handed to the playback path. We wait until playback is enabled and the current note has finished, we then move to wait (since song_rom is synchronous and needs 1 clk cycle to return data). We then read the ROM note, split into duration and note, and either load or transition to done (if duration is 0). We then stay in song_done until reset or a song change occurs. Therefore, we have a simple fetch-and-dispatch controller that sequences the note playback one ROM entry at a time.

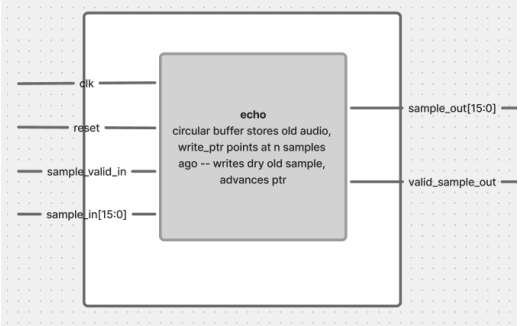
2, 3 – Weighted Harmonics (3 points) and ASDR Dynamics (4 points)



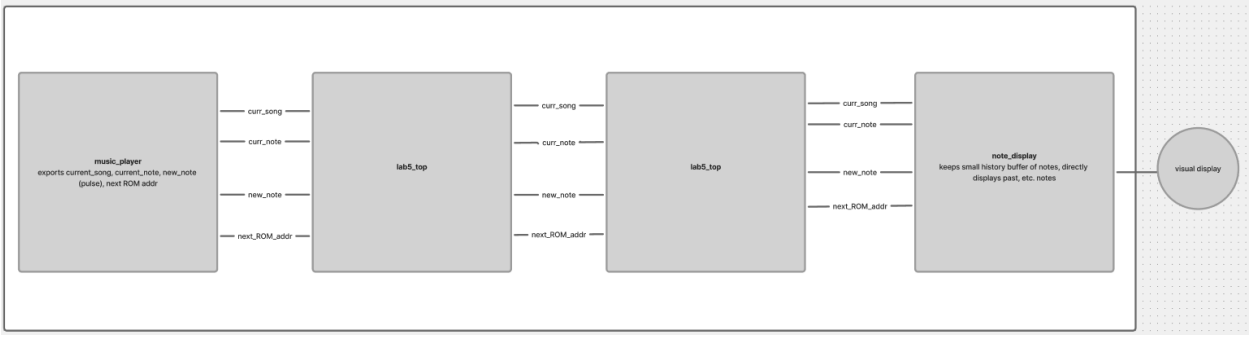


The ASDR envelope controls the note's amplitude over time. When a new note is triggered, the FSM leaves idle and enters ATTACK, where the amplitude rises linearly. It then moves to DECAY after reaching a maximum, where the amplitude falls exponentially to a sustained level, which triggers the SUSTAIN state. Once the note becomes inactive, the FSM transitions to RELEASE. In this implementation, the envelope level is multiplied by the harmonic waveform sample-by-sample, so the resulting audio has a shaped onset and fade-out rather than abrupt starts/stops.

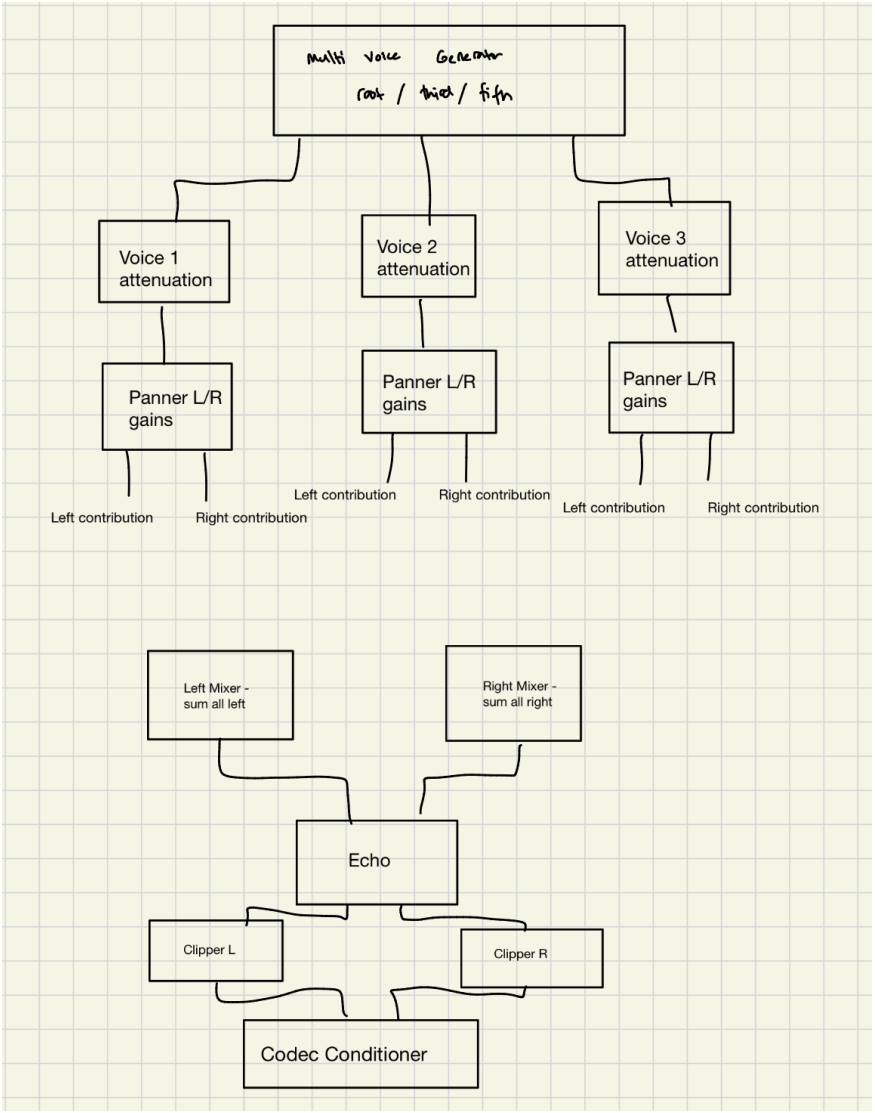
4 – Echo (2 points)



5 – Past, Future, and Present Note Display (4 points)



6 - Stereo Effects



TIMING TABLES:

Summary

- All intra-clock domains meet timing (100 MHz, 25 MHz, 48 MHz).
- All hold and pulse-width constraints are satisfied.
- All timing violations occur in a single inter-clock crossing:
    - 100 MHz -> 25 MHz
    - 24 failing endpoints
    - WNS = -2.711 ns

The design meets timing for all intra-clock domains, including the 100 MHz logic, 25 MHz display, and 48 MHz codec clocks. However, overall timing fails due to setup violations on clock domain crossings from the 100 MHz domain to the 25 MHz display domain. These violations are not due to excessive combinational delay, but actually from unsynchronized signals crossing between asynchronous clock domains.

Source report: `lab5/impl_1/lab5_top_timing_summary_routed.rpt`
Tool: Vivado 2019.2
Report date: March 16, 2026

*Vivado reports several generated clocks twice, once with and once without a `_1` suffix. The tables below collapse those duplicate entries and keep the worst-case values for each equivalent clock or clock pair.

Overall Timing Summary
Worst Negative Slack (WNS) | -2.711 ns
Total Negative Slack (TNS) | -58.219 ns
Setup failing endpoints | 24
Total setup endpoints | 2425
Worst Hold Slack (WHS) | 0.058 ns
Total Hold Slack (THS) | 0.000 ns
Hold failing endpoints | 0
Worst Pulse Width Slack (WPWS) | 2.000 ns
Pulse-width failing endpoints | 0
Timing met? | No

Clock Summary

Functional Clock	Period (ns)	Frequency (MHz)	Notes
System input	8.000	125.000	Board input clock
Main logic clock	10.000	100.000	Core processing
Display pixel clock	40.000	25.000	VGA/HDMI domain
Serializer clock	8.000	125.000	HDMI serializer
Codec clock	20.833	48.000	Audio codec

Intra-Clock Timing Table

Clock Domain	WNS (ns)	TNS (ns)	Failing Endpoints	WHS (ns)	Hold Fails	Status
Main logic (100 MHz)	0.096	0.000	0	0.131	0	Met
Display pixel (25 MHz)	21.892	0.000	0	0.148	0	Met

Codec (48 MHz)	18.799	0.000	0	0.491	0	Met

Inter-Clock Timing

From Domain	To Domain	WNS (ns)	TNS (ns)	Failing Endpoints	WHS (ns)	Hold Fails	Status
Display (25 MHz)	Main logic (100 MHz)	5.626	0.000	0	0.307	0	Met
Main logic (100 MHz)	Display (25 MHz)	-2.711	-58.219	24	0.500	0	Failing
Codec (48 MHz)	Codec (48 MHz)	18.819	0.000	0	0.351	0	Met

Worst Violating Path
Source clock: Main logic (100 MHz)
Destination clock: Display pixel (25 MHz)
Path type: Setup
Slack: -2.711 ns
Requirement: 10.000 ns
Data path delay: 12.119 ns
Logic levels: 12 (LUT6: 11, MUXF7: 1)
Violating endpoints (this crossing): 24

Report Warnings
Input ports without delay constraints: 6
Output ports without delay constraints: 18
Register/latch pins with multiple clocks: 1296
Unconstrained internal endpoints: 0
Combinational loops: 0